TA Instruments

Thermal Analysis & Rheology

THERMAL SOLUTIONS

PREDICTING PRINTED CIRCUIT BOARD DELAMINATION

PROBLEM

Delamination or separation of the layers in printed circuit boards during the manufacturing process (particularly wave soldering) is a leading cause of product failure. Hence, there is the need for a quick test which can predict failure before production.

SOLUTION

Thermomechanical Analysis (TMA), which measures dimensional change in materials with temperature, is an ideally suited technique for evaluating the onset of delamination in these materials. Figure 1 shows the TMA curve for a PC board subjected to the following temperature regimen - heating at 10°C/minute from 30°C to 260°C followed by an isothermal hold for 20 minutes [260°C is the typical temperature of a wave soldering bath]. Below 110°C (8 minutes) the matrix material is glassy and expands. At 110°C, a transition occurs (the glass transition) above which the matrix becomes more "rubbery" and expands at a more rapid rate. All of these characteristics can be readily quantified from the TMA curve as shown in Figure 1 and provide additional information valuable to proper processing and handling of the material. At 260°C, the TMA profile is initially flat (a slight creep occurs due to the force on the TMA probe) until delamination occurs, as clearly indicated by a sudden upward dimensional change. In the material in Figure 1, the time to delamination at 260°C is 5 minutes which was deemed to be unacceptable for normal processing. Figure 2 shows the results for a second PC board where the 15 minute delamination time was acceptable.

[Note: The specimens for this TMA test were 6.3mm x 6.3mm squares cut from the PC board and dried in an oven at 105°C for 2 hours to remove moisture. The TMA probe force was 0.05N. This TMA delamination test is currently being reviewed as an IPC standard test method (IPC-TM-650). The IPC procedure considers a delamination time greater than 10 minutes at 260°C as acceptable.]

Figure 1. MULTILAYER PCB

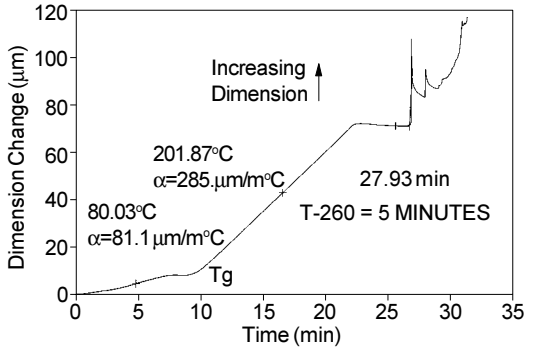
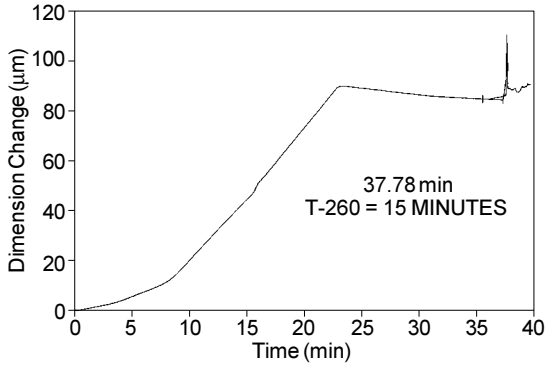


Figure 2. SURFACE LAYER PCB



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